

Winslow Adaptics

ASIC / PLD

To

FPGA Migration

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Alan Baker
Technical Development Manager
Winslow Adaptics
Tele: 01874 625555
Email: alan@winslowadaptics.com

ASIC / PLD to FPGA Migration

“Hello Winslow Adaptics, can I help you”

“ Well yes I hope so. You see the main printed circuit board of one of our best selling products was designed around an ASIC in a 68 pin PLCC package, and I am being told now that the fab plant can no longer manufacture it because they can no longer source the silicon at the right thickness – they called it progress”

“ Have you thought about replacing the ASIC with a FPGA”

“Well yes – do you do that sort of thing?”

“Yes we are quite experienced at that sort of thing. Have you chosen the FPGA that you want to use yet.”

“No. Can you give me some pointers as to what I should be considering?”

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This is not an uncommon conversation and it is not only ASICs which need replacing, early PLDs and FPGAs are now presenting sourcing problems. As the trend for extended product life continues to become more popular, the product development and the mid-life improvement programmes are quickly vanishing into the future. In procuring the components for the extended life product issues commonly occur when ASICs and early PLDs and CPLDs are involved. However as these devices are software configurable their replacement with currently available similar devices becomes a relatively easy process. For once the software required becomes the easier of the tasks to be undertaken. The development environments and design software which is now supplied to support these devices permit code development, testing and emulation to be achieved with ease. Integrating the new hardware device into an existing design, a design which was created a number of years ago using, what was then, cutting edge technology but now considered archaic can prove to be the problem area nowadays. However with the right choice of component and the adherence of some simple guidelines the problems can be easily overcome. Usually there are two areas which need to be considered, the choice of component and the design of an adapter which is generally required for the integration of the new device into the old design.

Selecting the Right Device

There are a number of areas which need to be considered when selecting a FPGA to replace an ageing logic design if it is going to integrate into the existing design with the minimum of disruption. It is highly unlikely that a perfect replacement can be found but, at least at the beginning of the integration phase, the problematic areas would have been previously identified.

Functionality

The functional capability of the new device is solely determined by the complexity of the original design. The point to note is that the device needs only to have the capability to meet the original design requirements and NOT the requirements of the original device. In many cases the original device has a far greater capability than was actually required, especially with respect to I/Os. Generally if the new device is matched to the design requirement then the resultant adapter design can be considerably easier. If the new device does have spare I/Os then consideration must be given as to what to do with them. Recommendations of some manufactures mean that spare I/Os need to be tied to a specific level whereas others can be left open circuit. The resultant design and power implications can be considerable if a significant number of spare I/Os need to be terminated.

Speed

The speed of any replacement device will undoubtedly be far superior to the original used due to the improvements in current manufacturing techniques. However the question should be asked as to whether the rest of the design can handle these increases in response and access times. Usually delays can be incorporated within the software of the new design, but it does need to be considered at the selection stage as not all devices can provide this type of code. Physical delays can be incorporated as part of the adapter design but are not recommended as a rule. One major area of mismatch usually occurs between the new program logic device and a the code storage device. See the notes on code storage.

Code Storage

A lot of existing ASIC and CPLD devices do not contain on chip memory for code storage and this is normally accomplished using a separate memory chip. Although these chips will have sufficient storage, the usual problem is the memory relatively slow access times which can provide a number of problems for the new device. There are normally three solutions: one is to abandon the memory chip and select an FPGA with on-board code storage, incorporate a compatible memory as part of the adapter or provide an adapter with a faster memory device to replace the existing code storage medium. Programming the memory will be considered as part of Design Considerations.

Core Voltage

The selection of the new device need not be constrained by the motherboard operating voltage. It is common place nowadays to include circuitry to adjust (usually down but not always) the in-coming voltage to the adapter to match the core voltage level (VccCore) of the new device. However see the notes on I/O voltage levels.

I/O Levels

Although it can be a relatively simple job to change the voltage used for the core supply of the new device, careful consideration must be given to the compatibility of the new device to the existing circuitry with respect to I/O levels. The common problem is that the existing design uses TTL levels and the new device is operates at either 3.3 or even 1.8 volts. Although the I/Os can be TTL 'tolerant' whereas inputs can operate with the existing levels it can mean that the output levels are not high enough to drive the existing circuits. Some devices allow the provision of I/O power

levels which are different to the core voltage, and in some cases it can be possible to provide drivers to adjust the new levels to an acceptable level, but is usually constrained to small numbers of outputs.

Package Type

There is no limitation on the type of package which can be used. In special circumstances designs based around die can be accomplished.

Package Size

Within reason the smallest physical package, which meets the requirements, should be selected however this will have an effect on the package pitch. This does not normally present issues unless a very fine pitch BGA is selected. The FPGA device is usually the main contributing factor with respect to the overall size of the adapter, which may or may not be design constraint.

Pitch

Device pitch is not usually a factor except with high count very fine pitch BGAs (0.4mm or less) which require special design techniques and manufacturing processes in order to be able to integrate the new device onto the motherboard.

Design Considerations

While considering which replacement device should be chosen it is advisable to look at some of the design issues and constraints around the adapter which will be required to integrate the new device into the old design. These considerations are likely to have an impact on the device selection.

Physical Size

It is generally a design requirement that the adapter design is no larger in area than the existing device. If this constraint is not applicable consideration will have to be given as to how the adapter is soldered onto the motherboard. If all interconnects cannot be accessed by soldering iron then all of the adapters (including those used in development for design proving) will have to solder using reflow. However constraints in the Z axis are not generally a problem. This can allow the adapter to utilize PoP (package on package) type techniques to provide additional surface area. Of course the size required will be directly proportional not only the size of the chosen FPGA but the ancillary circuits which will have to be included as part of the new design, i.e. Power supply, interface matching etc.

Environment

Although temperature, humidity and acceleration can provide constraints to design, the main factor which should be considered at design conception is vibration. The use of printed circuit substrates which are the same to the motherboard (with respect to coefficients of expansion) means that high LLC inter-connect techniques can be utilized without experiencing the reliability problems associated with those devices which use that inter-connect method. This will result in the adapter have a very low centre of gravity with respect to the motherboard and thus minimizing the effects of vibration.

The adapter can be supplied conformal coated but, in experience, this is best applied after the adapter has been installed on the motherboard to avoid contaminating the inter-connects of the adapter and the possibility of reaction between dis-similar coatings.

De-coupling

The decision needs to be made at design conception as to whether the adapter is to include the de-coupling devices for the new device, whether the existing de-coupling capacitors on the motherboard can be utilized or whether it will be a combination of the two design solutions. Much will depend on the existing design. In most cases there is sufficient de-coupling on the existing board, especially when the adapter utilizes ground and power planes as part of its design. In these cases a de-coupled Vcc input to the adapter is taken directly to a power plane. In the same manor the device power inputs are also connected directly to the power plane. Only where very little de-coupling on the motherboard has been provided or where the adapter does not utilize power planes should consideration be given to other de-coupling techniques.

Signals

In general no signal types present problems in the design of the adapter a because of the short inter-connect distances even very high speeds can be accomplished. Again balanced pairs and matched impedance designs are easily accomplished but need to be identified at design conception as there can influence the whole design. This is especially true with balanced pairs which must achieve equi-distant signal paths. Although most input signal will draw very little current care must be taken with certain types of outputs which can draw large currents (large with respect to the rest of the design). These do not present problems but must be indentified early so that correct tracking can be utilized in the design.

Power Supply

Small power supplies which utilize very few external components are readily available but care must be given to the power requirements of the new device, especially concerning I/Os as this can prove critical to the type/capability/power and thus size of the chosen supply.

Programming

The inclusion of the ability to program on board either the FPGA and or the memory chip is a desirable provision. This may have been impossible with the original design but the change of memory device and the introduction of a FPGA will undoubtedly change the method of programming and thus the type of interface which needs be provided. Usually the main problem which is encountered is the space available to include a suitable socket type interface and this has to be designed in from the beginning. Obviously the more modern types of programming interface are more desirable as they tend to use less circuits i.e. ST Micro SWIL as opposed to JTAG.

Special Requirements

One of the main advantages of using an adapter is that at the time of design special requirements can be incorporated. Quite often the new design can provide product improvement as well as solving supply issues and the adapter offers an excellent platform for this to be undertaken.

A Way Ahead

Not all of the above are individual mandatory requirements but if each point is at least considered then a successful outcome can be achieved. What we will have provided is a bridge, a means of travelling across the void left by component unavailability to a time when the problem can be resolved by re-design or product replacement. But what if this concept of bridging was applied at initial design conception? Could it be possible for foundations to left in designs for future bridges to be built across critical components? If it could then future obsolescence problems could be solved with greater ease and the phrase pro-active obsolescence management would be nearer to a reality.